

REMARKS

I. Overview of the Office Action

Claims 2, 12 and 20 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

Claims 1, 3-4, 11, 13-14, 18-19 and 21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Conley (U.S. Patent Application Publication No. 2002/0099904).

Claims 5-6, 8-10, 15 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Conley in view of Kim (U.S. Patent No. 6,381,176).

II. Statement of Substance of Interview

Applicants gratefully acknowledge an opportunity to teleconference with Examiner Rutz on September 26, 2008. The Examiner and Applicants discussed the rejection of claims 2, 12 and 20 under 35 U.S.C. § 112, first paragraph. As a result of this discussion, it is Applicants' understanding that claims 2, 12 and 20, as amended, overcome the rejection under 35 U.S.C. § 112, first paragraph. It is further Applicants' understanding that this ground of rejection of claims 2, 12 and 20 will be withdrawn.

It is respectfully submitted that the instant STATEMENT OF SUBSTANCE OF INTERVIEW complies with the requirements of 37 C.F.R. §§1.2 and 1.133 and MPEP §713.04.

III. Rejections of claims 2, 12 and 20 - 35 U.S.C. § 112

Claims 2, 12 and 20 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

Claims 2, 12 and 20 have been amended to alleviate Examiner's rejection under § 112, first paragraph. For example, Claim 2, as amended, recites: "wherein each physical block comprises: a first area, into which the data is written, and a second area, into which meta-information is written." The support for this amendment is found, for example, in paragraph 51 of the specification. Accordingly, it is respectfully requested this ground of rejection of claims 2, 12 and 20 be withdrawn.

IV. Prior Art Rejections - 35 U.S.C. § 102(b)

Claims 1, 3-4, 11, 13-14, 18-19 and 21 stand rejected under 35 U.S.C. 102(b) as being anticipated by Conley (U.S. Patent Application Publication No. 2002/0099904).

Claim 1 recites among other elements: “the flash memory controller is configured to write data and meta-information comprising flash memory state information comprising an indicator which indicates a state of the physical block as valid, deleted, or invalid, . . . and the flash memory controller is configured to perform a write operation for writing the data and the meta-information, comprising writing the valid indicator.”

Conley discloses updating data by programming the new data in unused pages of either the same or another block. (Abstract). When reading the data, the most recent pages of data are used and the older superceded pages of data are ignored. (Paragraph 48).

Each page may contain a field that provides an indication of its time of programming (time stamp). This allows the controller to determine, when reading the data from the memory, the relative ages of the pages of data that are assigned the same logical address. This involves a real-time clock. (Paragraphs 50, 51).

An output of a counter may be stored as the value of the field 43. When updating the data of a particular page in the original block PBN0, for example, the controller first reads the count stored in the field 43 of the page whose data are being updated, increments the count by one, and then writes that incremented count in the new block PBN1 as the field 43'. (Paragraph 51). The controller compares the counts in the fields 43 and 43' of pages having the same LBA and page offset. (Paragraph 52).

Alternatively, a single time stamp is recorded for each block, either as part of the block or elsewhere within the non-volatile memory, and is updated each time a page of data is written into the block. Data is then read from pages in an order of descending physical address, starting from the last page of the most recently updated block containing data pages having the same LBN. (Paragraph 56).

Therefore, Conley discloses searching for free pages in the block. If the free pages are not found, the data is written into the free pages of another block. The logical data is not changed for the old or the new block. Rather, the new data is identified by tracking the newest pages. The newest pages are tracked by (1) a time stamp; (2) a counter; (3) a memory location. The controller reads the pages from the memory and determines which pages, assigned to the same logical address, are new and which are old.

Conley does not teach or suggest writing meta-information for each page which comprises writing an indicator to indicate a state of the physical block as valid, deleted or invalid. Conley writes either (1) a time or (2) a counter for each page. In contrast, amended claim 1 requires each physical block to be identified as valid, invalid or deleted. Further, the writing of the valid indicator is performed for the memory state information of the physical block into which the writing is being currently performed, without changing the memory state information of the old block.

Because Conley does not teach or suggest at least “the flash memory controller is configured to write data and meta-information comprising flash memory state information comprising an indicator which indicates a state of the physical block as valid, deleted, or invalid, ... and the flash memory controller is configured to perform a write operation for writing the data and the meta-information, comprising writing the valid indicator,” **claim 1 and dependent claims 2-4** distinguish patentably over Conley.

Claim 11 recites features similar to, although not necessarily coextensive with, the features argued above with respect to claim 1. Accordingly, the arguments presented with respect to claim 1 apply with equal force here. For at least analogous exemplary reasons, therefore, **claim 11 and dependent claims 12-14** distinguish patentably over Conley.

Claim 18 recites features similar to, although not necessarily coextensive with, the features argued above with respect to claim 1. Accordingly, the arguments presented with respect to claim 1 apply with equal force here. For at least analogous exemplary reasons, therefore, **claim 11 and dependent claims 19-21** distinguish patentably over Conley.

V. Claim Rejections - 35 U.S.C. § 103

Claims 5, 6, 8-10, 15 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Conley in view of Kim (U.S. Patent No. 6,381,176).

Applicants have already demonstrated that Conley does not teach or suggest all of the features of the independent claims. Kim does not cure any deficiencies of Conley. Therefore, **claims 5, 6, 8-10, 15 and 17** distinguish patentably and unobviously over Conley and Kim, taken singularly or in combination, at least by virtue of their dependencies.

VI. New Claims

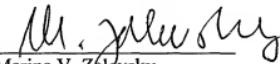
Applicants add new claims 22-25 to further define the invention. **Claims 22-25** are patentable at least by virtue of their dependencies and for additional features recited therein. No new subject matter has been entered.

VII. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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